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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BELL, PAUL A	

ART UNIT	PAPER NUMBER
2675	24

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/448,756	KOYMA ET AL.	
	Examiner	Art Unit	
	PAUL A BELL	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. *08/803,217* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The abstract of the disclosure is objected to because it is not related directed towards the present claims in this continuation. Correction is required. See MPEP § 608.01(b).

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto (5,323,042) in view of Adachi et al. (5,631,664) and Asars (4,114,070).

With regard to claim 1 Matsumoto teaches an active matrix type display device comprising: a substrate having an insulating surface , a plurality of pixel electrodes arranged in a matrix form over said substrate , a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor (column 1, lines 5-12 figure 1, item 12, figure 4, item 6); and a driver circuit comprising a plurality of

thin film transistors for driving said plurality of switching elements (figure 1, item 13, figure 4, item 2 and 3), wherein each of said plurality of thin film transistors comprises a crystallized semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystallized semiconductor layer and a gate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22).

Matsumoto does not teach " a display medium comprising an emissive material and capable of electrically changing luminous strength disposed at each of said pixel electrodes" . Matsumoto instead teaches a display medium being an liquid crystal which is not an "emissive material".

Adachi et al. teaches a preference for EL or electroluminescence material which is a "emissive material" over liquid crystal material (See Adachi et al. column 1, lines 37-66).

Asars teaches with regards to using EL or LCD material in a matrix that the, "The basic electronic control circuitry for both panels is essentially the same", (col 2, lines 50-53).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Matsumoto display medium to be EL instead of LC because Adachi et al. provided the suggestion and motivation to substitute EL for LC(See Adachi et al. column 1, lines 37-66) and still further Asars provided the "reasonable expectation of success" in making the change (See Asars col 2, lines 50-53).

With regard to claim 2 Matsumoto as modified by Adachi et al. and Asars teaches wherein said gate electrode is located over said semiconductor layer (See Matsumoto figure 1, items 26 and 11).

With regards to claim 3 Matsumoto as modified by Adachi et al. and Asars teaches wherein all of said plurality of thin film transistors are p-type (See Matsumoto column 5, line 67-68).

With regard to claim 4 Matsumoto as modified by Adachi et al. and Asars teaches wherein all of said plurality of thin film transistors are n-type (See Matsumoto column 5, line 67-68).

With regard to claim 5 Matsumoto as modified by Adachi et al. and Asars teaches wherein said substrate is a glass substrate (See Matsumoto column 3, line 3).

With regard to claim 6 Matsumoto as modified by Adachi et al. and Asars teaches wherein said crystallized semiconductor layer comprises silicon (See Matsumoto column 3, line 60).

With regard to claim 7 Matsumoto as modified by Adachi et al. and Asars teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor (See Matsumoto column 1, lines 5-12 figure 1, item 12, figure 4, items 6 and 7), and a driver circuit comprising a plurality of thin film transistors for driving

said plurality of switching elements (See Matsumoto figure 1, item 13, figure 4, item 2 and 3), wherein each of said plurality of thin film transistors comprises a crystallized semiconductor layer (See Matsumoto column 3, lines 59-64), a gate insulating film adjacent to said crystallized semiconductor layer and a gate electrode adjacent to said gate insulating film (See Matsumoto figure 1, items 26, 24, and 22) , wherein said crystallized semiconductor layer has source and drain regions and at least one lightly doped region (See Matsumoto column 3, lines 7-17).

With regard to claim 8 Matsumoto as modified by Adachi et al. and Asars teaches wherein said substrate is a glass substrate (See Matsumoto column 3, line 3).

With regard to claim 9 Matsumoto as modified by Adachi et al. and Asars teaches wherein said source and drain regions and said at least one lightly doped region are doped with phosphorus (See Matsumoto column 4, lines 1-35).

With regard to claim 10 Matsumoto as modified by Adachi et al. and Asars teaches

wherein said source and drain regions and said at least one lightly doped region are doped with boron (See Matsumoto column 4, lines 1-35).

With regard to claim 11 Matsumoto teaches as modified by Adachi et al. and Asars wherein said gate electrode is located over said semiconductor layer (See Matsumoto figure 1, items 26 and 11) .

With regard to claim 12 Matsumoto as modified by Adachi et al. and Asars teaches wherein said crystallized semiconductor layer comprises silicon (See Matsumoto column 3, line 60).

With regard to claim 13 Matsumoto as modified by Adachi et al. and Asars teaches an active matrix type display device comprising: a substrate having an insulating surface; a plurality of pixel electrodes arranged in a matrix form over said substrate; a plurality of switching elements operationally connected to said pixel electrodes (See Matsumoto column 1, lines 5-12 figure 1, item 12, figure 4, item 7), each of said switching elements comprising a thin film transistor (See Matsumoto figure 1, item 12, figure 4, item 6), and a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor (See Matsumoto column 2, line 68), wherein each of said n-channel and p-channel type thin film transistors comprises a crystallized semiconductor layer (See Matsumoto column 3, lines 59-64), a gate insulating film adjacent to said crystallized semiconductor layer and a gate electrode adjacent to said gate insulating film (See Matsumoto figure 1, items 26, 24, and 22).

With regard to claim 14 Matsumoto as modified by Adachi et al. and Asars teaches wherein aid substrate is a glass substrate (See Matsumoto column 3, line 3).

With regard to claim 15 Matsumoto as modified by Adachi et al. and Asars teaches wherein said gate electrode is located over said semiconductor layer (See Matsumoto figure 1, items 26 and 11) .

With regard to claim 16 Matsumoto as modified by Adachi et al. and Asars teaches wherein said crystallized semiconductor layer comprises silicon (See Matsumoto column 3, line 60).

With regard to claim 17 Matsumoto as modified by Adachi et al. and Asars teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (See Matsumoto column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (See Matsumoto figure 1, item 12, figure 4, item 6), and a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor (See Matsumoto column 2, line 68), each of said thin film transistors comprising a crystallized semiconductor layer (See Matsumoto column 3, lines 59-64), a gate insulating film adjacent to said crystallized semiconductor layer and a gate electrode adjacent to said gate insulating film (See Matsumoto figure 1, items 26, 24, and 22), wherein said crystallized semiconductor layer has source and drain regions and at least one lightly doped region (See Matsumoto column 3, lines 7-17).

With regard to claim 18 Matsumoto as modified by Adachi et al. and Asars teaches wherein said substrate is a glass substrate (See Matsumoto column 3, line 3).

With regard to claim 19 Matsumoto teaches as modified by Adachi et al. and Asars an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (See Matsumoto column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film

transistor (See Matsumoto figure 1, item 12, figure 4, item 7), and a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements (See Matsumoto figure 4, items 2 and 3), wherein each of the film transistors of said switching elements and said driver circuit comprises a crystallized semiconductor layer (See Matsumoto column 3, lines 59-64), a gate insulating film adjacent to said crystallized semiconductor layer and agate electrode adjacent to said gate insulating film (See Matsumoto figure 1, items 26, 24, and 22).

With regard to claim 20 Matsumoto as modified by Adachi et al. and Asars teaches wherein said gate electrode is located over said semiconductor layer (See Matsumoto figure 1, items 26 and 11) .

With regard to claim 21 Matsumoto as modified by Adachi et al. and Asars teaches wherein all of said plurality of thin film transistors are p-type (See Matsumoto column 5, line 67-68).

With regard to claim 22 Matsumoto as modified by Adachi et al. and Asars teaches wherein all of said plurality of thin film transistors are n-type (See Matsumoto column 5, line 67-68).

With regard to claim 23 Matsumoto as modified by Adachi et al. and Asars teaches wherein said substrate is a glass substrate (See Matsumoto column 3, line 3).

With regard to claim 24 Matsumoto as modified by Adachi et al. and Asars teaches wherein said crystallized semiconductor layer comprises silicon (See Matsumoto column 3, line 60).

With regard to claim 25 Matsumoto as modified by Adachi et al. and Asars teaches In regards to claim 25 An active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (See Matsumoto column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (See Matsumoto figure 1, item 12, figure 4, item 7), and a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements (See Matsumoto figure 4, items 2 and 3), wherein each of the thin film transistors of the switching elements and the driver circuit comprises a crystallized semiconductor layer (See Matsumoto column 3, lines 59-64), a gate insulating film adjacent to said crystallized semiconductor layer, and a gate electrode adjacent to said gate insulating film (See Matsumoto figure 1, items 26, 24, and 22), wherein said crystallized semiconductor layer has source and drain regions and at least one lightly doped region (See Matsumoto column 3, lines 7-17).

With regard to claim 26 Matsumoto as modified by Adachi et al. and Asars teaches wherein said substrate is a glass substrate (See Matsumoto column 3, line 3).

With regard to claim 27 Matsumoto as modified by Adachi et al. and Asars teaches wherein said source and drain regions and said at least one lightly doped region are doped with phosphorus (See Matsumoto column 4, lines 1-35).

With regard to claim 28 Matsumoto as modified by Adachi et al. and Asars teaches wherein said source and drain regions and said at least one lightly doped region are doped with boron (See Matsumoto column 4, lines 1-35).

With regard to claim 29 Matsumoto as modified by Adachi et al. and Asars teaches wherein said gate electrode is located over said semiconductor layer (See Matsumoto figure 1, items 26 and 11) .

With regard to claim 30 Matsumoto as modified by Adachi et al. and Asars teaches In regards to claim 30 wherein said crystallized semiconductor layer comprises silicon (See Matsumoto column 3, line 60).

With regard to claim 31 Matsumoto as modified by Adachi et al. and Asars teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (See Matsumoto column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (See Matsumoto figure 1, item 12, figure 4, item 7), and a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor (See Matsumoto column 2, line 68), wherein each of the film transistors of the switching elements and said n-channel and p-channel type thin film transistors comprises a crystallized semiconductor layer (See Matsumoto column 3, lines 59-64), a gate insulating film adjacent to

said crystallized semiconductor layer and a gate electrode adjacent to said gate insulating film (See Matsumoto figure 1, items 26, 24, and 22).

With regard to claim 32 Matsumoto as modified by Adachi et al. and Asars teaches wherein said substrate is a glass substrate (See Matsumoto column 3, line 3).

With regard to claim 33 Matsumoto as modified by Adachi et al. and Asars teaches wherein said gate electrode is located over said semiconductor layer (figure 1, items 26 and 11) .

With regard to claim 34 Matsumoto as modified by Adachi et al. and Asars teaches wherein said crystallized semiconductor layer comprises silicon (See Matsumoto column 3, line 60).

With regard to claim 35 Matsumoto as modified by Adachi et al. and Asars teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (See Matsumoto column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (See Matsumoto figure 1, item 12, figure 4, item 7), and a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor (See Matsumoto column 2, line 68), wherein each of the film transistors of the switching elements and said n-channel and p-channel type thin film transistors comprises a crystallized semiconductor layer (See Matsumoto column 3, lines 59-64), a gate insulating film adjacent to said crystallized semiconductor layer and a gate electrode adjacent to said gate insulating film (See Matsumoto

figure 1, items 26, 24, and 22), and said crystallized semiconductor layer has source and drain regions and at least one lightly doped region (See Matsumoto column 3, lines 7-17).

With regard to claim 36 Matsumoto as modified by Adachi et al. and Asars teaches wherein said substrate is a glass substrate (See Matsumoto column 3, line 3).

With regard to claim 37 Matsumoto as modified by Adachi et al. and Asars teaches wherein said crystallized semiconductor layer comprises silicon (See Matsumoto column 3, line 60).

With regard to claim 38 Matsumoto as modified by Adachi et al. and Asars teaches wherein said crystallized semiconductor layer comprises silicon (See Matsumoto column 3, line 60).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Bell whose telephone number is (703) 306-3019. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to: Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to: (703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Paul Bell
Art unit 2675
27 October 2003

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600